

## ABSTRACT

A membrane switch circuit layout and method for producing a membrane switch circuit layout are disclosed. The membrane switch circuit layout may have two or more membrane layers. Each membrane has a top surface and a bottom surface. A conductive circuit trace is printed on the top surface of each membrane. The membrane layers are placed in a stack with each top membrane having thru-holes selectively cut there through. Thus, for example, in a layout having two membrane layers, the first membrane is positioned beneath the second membrane and the second membrane has thru-holes cut there through. Conductive ink may be pressed through the thru-holes to provide electrical connection between the circuit traces printed on the membrane layers. An adhesive may be placed between the membrane layers as either adhesive printed on one of the membrane layers or as an additional layer.

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